WHAT IS CLAIMED IS:

1. A semiconductor device having a semiconductor resistance element, comprising:

a compound semiconductor substrate;

an n-type semiconductor resistance region formed in the surface of said compound semiconductor substrate; and

a p-type buried region provided between said n-type semiconductor resistance region and a substrate region formed by said compound semiconductor substrate.

2. A semiconductor device having a semiconductor resistance element according to claim 1, wherein said compound semiconductor substrate is a semi-insulating substrate.

3. A semiconductor device having a semiconductor resistance element according to claim 1, wherein an acceptor concentration in said p-type buried region is selected to be higher than an acceptor concentration in said substrate region and to be lower than a donor concentration in said n-type semiconductor resistance region.

4. A semiconductor device having a semiconductor resistance element according to claim 1, wherein said p-type buried region is perfectly depleted.

5. A semiconductor device having a semiconductor resistance element according to claim 1, wherein said n-type semiconductor resistance region and said p-type buried region are formed with a self-alignment positional relationship kept therebetween.

6. A method of fabricating a semiconductor device having a semiconductor resistance element,

comprising:

a step of doping an n-type impurity in a selected region in the surface of a semi-insulating compound semiconductor substrate via a first mask layer formed on the surface of the compound semiconductor substrate, to form an n-type impurity doped region;

a step of doping, after or before said step of forming the n-type impurity doped region, a p-type impurity in the surface of said compound semiconductor substrate via a second mask layer formed on the surface of said compound semiconductor substrate, to form a p-type impurity doped region;

a step of heat-treating the compound semiconductor substrate, to activate the impurities in the n-type impurity doped region and the p-type impurity doped region, thereby forming an n-type semiconductor resistance region, and also forming a p-type buried region between the n-type semiconductor resistance region and a substrate region of the semiconductor substrate in such a manner as to bring the p-type buried region into contact with the n-type semiconductor resistance region; and

a step of forming ohmic electrodes in the semiconductor resistance region.

7. A method of fabricating a semiconductor device having a semiconductor resistance element according to claim 6, wherein the n-type impurity doped region and the p-type impurity doped region are formed in self-alignment by commonly using one mask layer as the first and second mask layers.